Title
An ultrafast phase-change logic device driven by melting processes

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Abstract

The ultra-high demand for *faster* computers is currently tackled by traditional methods such as size-scaling (for increasing the number of devices), but this is rapidly becoming almost impossible, due to physical and lithographic limitations. To boost the speed of computers without increasing the number of logic devices, one of the most feasible solutions is to increase the *number of operations* performed by a device, which is largely impossible to achieve using current silicon-based logic devices. Multiple operations in phase-change-based logic devices have been achieved using crystallization; however, they can achieve mostly speeds of several *100's* of nanoseconds. A difficulty also arises from the trade-off between the speed of crystallization and long-term stability of the amorphous phase. We here instead control the process of *melting* through "pre-melting disordering" effects, while maintaining the superior advantage of phase-change-based logic devices over silicon-based logic devices. A melting speed of just *900 picoseconds* was achieved to perform multiple Boolean algebraic operations (e.g. NOR and NOT). *Ab initio* molecular-dynamics simulations and *in situ* electrical characterization revealed the origin (i.e. bond-buckling of atoms) and kinetics (e.g. discontinuous-like behavior) of melting through "pre-melting disordering", which were key to increasing the melting speeds. By a subtle investigation of the well-characterized phase-transition behavior, this simple method provides an elegant solution to boost significantly the speed of phase-change-based 'in-memory' logic devices, thus paving the way for achieving computers that can perform computations approaching *terahertz* processing rates.

Significance Statement

The ever-increasing demand for *faster* computers is tackled by reducing the size of devices, but this is becoming almost impossible to continue. To improve the speed of computers, a solution is to increase the *number of operations* performed per device. Numerous operations in phase-change-based 'in-memory' logic devices have previously been achieved using crystallization, but they show *slow* speeds, mostly due to a trade-off between the crystallization speed and stability of the initialized-glassy states. Here, we instead control *melting* processes to perform logic operations. *Ultrafast* melting speeds and diverse operations were achieved. Computer simulations and electrical measurements show the *origin* and *kinetics* of melting. These advances open the doorway for developing computers that can perform calculations at *well beyond* current-processing rates.

Keywords
Computing, logic devices, melting, phase-change materials

Classification
Applied physical sciences

Main text/body

The extremely high and ever-increasing demand for *faster* computers is currently addressed by traditional methods, such as miniaturization (in order to increase the number of devices), but this is rapidly becoming almost impossible, due to physical and lithographic constraints (1-4). The speed of computers is known to be determined almost solely by the performance of logic devices, i.e. their *speed* and *number*, which control most computations (or processes) in computers (5). Logic devices are mostly required to operate around 1 ns for achieving fast computations, and to transfer information between alternate devices, such as random-access memories, without delays (5). To increase the speed of computers without increasing the number of logic devices, one of the most feasible methods is to increase the *number of operations* performed by a device, which is largely unachievable using current silicon-based logic devices (6,7).

Multiple operations in a logic device are currently best achieved using devices comprised of phase-change non-volatile memory materials – based on the reversible and multi-level switching of a phase-change material (PCM) between crystalline and glassy states having a contrast in physical properties, e.g. electrical resistivity (8,9) – which can perform more than *three times* the number of operations than can silicon-based logic devices (10,11). They also have the advantage of in-memory operation: the logical state is stored in a non-volatile manner in the cell itself. Multiple operations in phase-change-based logic devices have been achieved using crystallization; however, crystallization is a slow process and this approach can achieve mostly speeds of several *hundreds* of nanoseconds (10,11). A difficulty arises from the trade-off between increasing the speed of crystallization and, at the same time, extending the long-term (non-volatile) stability of the initialized glassy state in

order to avoid spontaneous crystallization causing corruption of the initial logic state (12).

We here instead control the processes on *melting* via "pre-melting disordering" phenomena, while maintaining the superior advantage of the phase-change-based logic devices over silicon-based logic devices, as well as avoiding the stability drawbacks in previous crystallization-based logic operations by employing a stable crystalline phase, rather than the thermally-vulnerable amorphous phase, as the initial logic state. Ultrafast melting speeds were achieved, as well as multiple Boolean algebraic operations. *Ab initio* molecular-dynamics simulations and *in situ* electrical characterization revealed the microscopic origin and transient kinetics of melting through "pre-melting disordering" phenomena, respectively, which were observed to be key to increasing the melting speeds.

We find that Ge-Sb-Te alloys (e.g. $Ge_2Sb_2Te_5$ or GST), which are technologically important for phase-change non-volatile information storage, provide a nearly ideal system for achieving Boolean algebraic operations, and for tracking the transient behavior of melting or solid-to-liquid (*s*-to-*l*) transitions. This allows for the precise and systematic control of disorder in a crystalline solid via the use of a weak electric field/electrical 'priming' pulse, which is applied to a test cell, comprising a 90-nm wide cylinder of GST sandwiched between two TiW electrodes (see Methods and Supplementary Information (SI) Appendix: Fig. S1). Such "priming" effects are largely difficult to detect through conventional material characterization, for instance electron diffraction of the gradual changes in the structure of GST caused by multiple-electrical pulses (13), but are evidenced in this study via a simple approach comprising *in situ* electrical-conductivity measurements of both pronounced and fast variations in the GST structure upon applying a single electrical pulse. Such high

electrical sensitivity is the key to revealing the microscopic origin of an *s*-to-*l* transition in this material.

We have shown that a GST cell shows multiple Boolean algebraic operations via control of the switching from crystalline to glassy states. By applying a 'double-pulse' priming/switching-excitation scheme, a single cell can exhibit two combinations of electrical-resistance levels: a) an *L-H-H-H* resistance combination resulting from LO-LO, LO-HI, HI-LO and HI-HI pulses with no separation (Fig. 1A); and b) an *L-L-L-H* resistance combination resulting from the same set of pulses, but with a separation of t = 100 ns (Fig. 1B). *L* and *H* refer to low- and high-resistance levels, which are below and above a reference resistance level, here taken to be $R = 0.7$ MΩ, while LO and HI denote low- and high-voltage pulses, respectively (Figs. 1C, D). By representing the *L* and *H* resistance levels, and the causative HI and LO pulses, as the binary numbers '1' and '0', $\neg(x \vee y)$/NOR and $\neg(x \wedge y)$/NAND operations are demonstrated, respectively (Figs. 1C, D). It should be noted that this is also twice the number of operations observed in the 'non-priming' excitation scheme (using only HI pulses), (which can only show NAND operation both with and without a separation) (see SI Appendix: Figs. S18). Furthermore, single LO/HI pulses and their corresponding resulting *L*- and *H*-resistance levels can be employed to generate a $\neg x$/NOT operation (Fig. 1E). Such control is derived from a dependence of the cell resistance on the voltage, length and separation of the electrical pulses (see SI Appendix: Figs. S14-S16). Ultimately, a modular expansion of such a method can facilitate even greater control of the resistance levels, as new material/device structures are developed with a higher number of resistance levels and resistance-level combinations (11,14).

The GST cells have been shown to exhibit ultra-fast Boolean algebraic operations via boosting the energy delivered by electrical-pulse excitation. Generally, a fast

crystal-to-glass transition is realized through applying a high input energy, which promotes rapid structural disordering in GST (15-17). As predicted, the GST cell exhibits faster switching from the crystalline to glassy states for both NOR and NOT operations as the amplitudes of the LO/HI electrical pulses are increased from 1.55 V/1.70 V to 4.6 V/5.0 V (Fig. 1F). Remarkably, such operations can be achieved with electrical pulses as short as t = 400/500 ps or a total pulse length of 900 ps (Fig. 1F) – which is *two orders* of magnitude shorter than those needed to manipulate the alternative 'crystallization' excitation schemes previously used for Boolean algebraic operations in GST (10,11). It should be noted that this is also as short/shorter than those obtained for the cells in the 'non-priming' excitation scheme (of 5.0 V and (minimum) 1 ns) (see SI Appendix: Figs. S18,S17). In addition, the energy density needed to perform Boolean algebraic operations can be estimated by a simple calculation of the area under the pulse waveforms used (i.e. the sum of their amplitude-length products). In the worst-case scenario, to perform Boolean algebraic operations with two high-voltage (input) pulses, the energy density needed for the 'priming' excitation scheme is given by $2 \times (5.0 \times 0.5\times10^{-9}) = 5$ nJ/A, which is *139* times lower than the 'crystallization' excitation scheme (that is given by $2 \times (2.4 \times 70\times10^{-9} + 1.5 \times 120\times10^{-9}) = 696$ nJ/A) (10). This is also two times lower than for the 'non-priming' excitation scheme (which is given by $2 \times 5.0 \times 1.0\times10^{-9} = 10$ nJ/A). This demonstrates the potential for exploiting crystal-to-glass kinetics for ultrafast logic applications, although the device performance and (Boolean algebraic) implementation of a GST cell, such as the power consumption, temporal resistance drift and sequential operation, can be enhanced/optimized further (see Supporting Information).

We investigated the transient characteristics of an *s*-to-*l* transition occurring during the Boolean algebraic operations by evaluating the *in situ* electrical conductance of a GST cell upon electrical-pulse excitation. The cell, initially in the crystalline state, was excited with an onset voltage, e.g. V_{on} ~ 1.5 V (similar to the amplitudes of the low-voltage pulses that were key to achieving the Boolean algebraic operations in Figs. 1C and D), which induces the onset of an *s*-to-*l* transition by locally heating the material above its melting temperature, T_m, via Joule heating (18); the V_{on} value was determined via the dependence of the current flow on the constant voltage applied to the cell (Fig. 2A, top right). In general, most metals or materials exhibit a transition from the solid to a liquid/melt state that yields an increase in the electrical conductivity (19,20). By applying an electrical pulse with an amplitude of around V_{on} (e.g. V = 1.47 or 1.50 V), we find that the GST cell exhibits a similar transition (as manifested by a pronounced rise in the current flow or electrical conductivity), which is mostly discontinuous-like – it does not occur instantly, but rather at longer time scales (t = 1.3 μs or 1.8 μs) (Fig. 2A, left). In addition, such a 'delay' or 'growth of disorder' prior to an *s*-to-*l* transition is not observed when either a low- or high-voltage pulse is applied (e.g. V = 1.10 or 1.90 V), i.e. the transition has not occurred or has taken place almost immediately, respectively, meaning that such phenomena occur only around T_m.

To investigate the origin of the growth of disorder, the structural disordering of a crystalline GST model at varying temperatures was examined. Recently, we have investigated such disordering essentially at and after an *s*-to-*l* transition in GST using AIMD simulations, which have provided new structural and functional insights into the microscopic processes involved (17). We illustrate the power of this approach by examining the structural changes prior to an *s*-to-*l* transition in a GST model,

comprising twenty-two Ge, twenty-two Sb, and fifty-five Te atoms, heated between *T* = 800 and 900 K (see Methods); these parameters were chosen, based on a correlation between the temperature, size and time scale of the simulational studies (see Supporting Information). Generally, during an *s*-to-*l* transition, a sharp decrease would occur in the number of ordered structural units, *viz.* fourfold rings (which are a structural motif of the metastable rocksalt crystal structure of GST), due to the high level of structural disordering characteristic of the liquid/melt phase (20) (Fig. 2B, right). Indeed, the time evolution of the decay in the number of fourfold rings in the GST models at intermediate temperatures (e.g. *T* = 825 and 850 K) exhibits such transitional characteristics, but only after a (growth of disorder) time of around *t* = 50 ps (Fig. 2B, left), similar to those observed experimentally, although the time scale is shorter due to the small GST model employed (Fig. 2A, see also Supporting Information). Moreover, pronounced fluctuations in the number of fourfold rings are observed during the growth of disorder, suggesting the emergence of a premonitory structural disordering.

During the growth of disorder, we found that the GST model exhibits a repeated stretching or "buckling" of the bonds within clusters of atoms, *viz.* the formation and annihilation of fourfold rings (Fig. 2C), while preserving the essence of crystalline order, which is largely independent of the model size, structural definition and starting configuration employed (see Supporting Information). We thus refer to this process as 'pre-melting disordering' (PD). Such disordering seems to be enabled by the intrinsic ability of the constituent atoms to occupy lower-coordinated sites in the liquid/melt phase than in the solid phase (21,22) (see Supporting Information). It should be noted that the PD phenomenon can be affected by the intrinsic disorder generated by thermal excitations, e.g. vibrational modes and point defects, or grain

boundaries, although they should yield similar changes in the material properties that accelerate the approach to an *s*-to-*l* transition, regardless of the crystalline structure that remains until the transition itself (23,24).

The PD phenomenon allows for the precise control of an *s*-to-*l* transition in a GST model/cell. In the simulations, the preheated GST model shows a much faster onset of such a transition (t ~ 10 ps) than a non-preheated GST model when melted at T = 875 K (t ~ 40 ps); the former is preheated at T = 825 K for ~ 35 ps prior to the melting at T = 875 K, while the latter is melted solely at T = 875 K (Fig. 3A). In addition, including the preheating time, the preheated model requires an overall time of t ~ 40 ps to complete an *s*-to-*l* transition, which is almost identical to that required by the non-preheated model, meaning that a similar transitional behavior (or outcome) can be achieved via two different excitation schemes (Fig. 3A, top right) – this can not only allow the Boolean algebraic operations, but also save energy (during preheating). The same phenomena are observed experimentally for the electrically primed and non-primed GST cells – they exhibit switching from the crystal to glass states using electrical pulses with lengths of t = 22 (7) ns including (excluding) the priming pulse, and t = 25 ns, respectively (Fig. 3B). That is, the switching speed of the cells can be altered, which confirms that such schemes could be applied to practical device operations. In addition, Figs. 3A and B show that, by preheating the models/cells using a simple priming method, the melting times can be reduced by more than *3.5 times* compared to not preheating the models/cells. Furthermore, the switching voltage (in the range V = 3.00 V to 1.55 V) and time (in the range t = 25 ns to 5 ns) decrease with an increase in the amplitude (V = 1.35 V to 1.75 V) and length (t = 5 ns to 20 ns) of a priming pulse (Figs. 3C, D). This indicates that the degree of

PD can be controlled and tuned for achieving multiple Boolean algebraic operations, and possibly even completely new applications.

Both experimental and simulational results suggest that fast, multiple, and low-power Boolean algebraic operations may stem from the cooperative movement of atoms during growth of disorder/priming, leading to a rapid, tunable, and low-energy formation of different glassy structures. At intermediate (high) temperatures, a large (much larger) buckling of bonds of clusters of atoms, evident from the AIMD simulations, will promote (boost) atomic diffusion, which is required for structural disordering. This phenomenon would explain both the observed fast switching, and also the multiple electrical-resistance levels and low power consumption seen in the GST cells.

The ‘priming’ scheme can provide an excellent approach for performing Boolean algebraic operations. The ‘priming’ scheme can avoid spontaneous crystallization of the initial logic state. Prior to performing the logic operations using the ‘crystallization’ scheme, the cell needs to be initialized to the amorphous state, and after the logic operations, the cell mostly needs to be re-initialized back to the amorphous state to stand by for the next logic operation (10,11). In contrast, prior to/after performing the logic operation using the ‘priming’ scheme, the cell needs to be initialized/re-initialized back to the crystalline state, and thus, the ‘priming’ scheme can perform logic operations using *stable* initial crystallization states, and therefore does not suffer from the unavoidable problem of spontaneous transformation (crystallization) of the initial state plaguing the ‘crystallization’ logic scheme.

In addition, another advantage of the ‘priming’ scheme concerns resistance drift in the amorphous state (see Supporting Information). Since the initialized state is

always the crystalline state, this will not suffer from resistance drift and hence time-dependent corruption of the initial state, in marked contrast to the case of the previous 'crystallization' scheme (10,11), especially if the reference resistance level of assigning the logical state is used. The fact that the final amorphous state could suffer from eventual resistance drift with time should not be too much of a problem as long as the logic state is always read out immediately after switching.

Furthermore, the 'priming' scheme can allow a much simpler way of reading out the logic outputs than the 'crystallization' scheme. In the 'crystallization' scheme, the logical state is mostly read out by using a final "confirm" pulse (10). In contrast, in the 'priming' scheme, the logical state can be read out by just using a reference level, which is much simpler (and quicker). The 'priming' scheme can also perform all logic operations using just one cell, rather than the two cells employed by the 'crystallization' scheme (11).

In general, apart from the input energy, the melting kinetics of a solid depend strongly on the strength of bonds between the atoms (25), and thus one interesting avenue for future investigation might be to examine the transient behavior during an *s*-to-*l* transition of alternative solid-state or phase-change materials with different structural characteristics, which could display varying PD phenomena. Indeed, it may be fruitful to study the glassy forms of a phase-change material, where local structural variability, particularly in the strength of bonds, could yield a less pronounced T_m. These future studies would facilitate the use of various types of materials/device structures, in isolation and in combination, to open up new opportunities for optimizing the performance of phase-change-based, in-memory logic devices.

Methods

a. Cell structure

SI Appendix: Fig. S1 shows the structure of a test cell in the lateral or cross-sectional plane, wherein the cell is deposited on an SiO_2-on-Si substrate. The cell has a pore-like structure comprising a 35 nm thick phase-change (PC) material layer ($Ge_2Sb_2Te_5$ or GST), which is sandwiched between the top and bottom electrodes (TiW) with thicknesses of 200 nm. The phase-change material is confined in a 90 nm-wide via formed by an insulating layer (SiO_2) with a thickness of 35 nm. The electrodes are used to connect the cell to the external circuitry for the electrical measurements, while the insulating layer provides the electrical and thermal insulation.

b. Device fabrication

The cells were fabricated using an integrative conventional lithography and nanopatterning technique. Each patterning step was accomplished using 365 nm photolithography (Cannon) or electron-beam lithography (JEOL), followed by the material-deposition and lift-off processes. All of the materials were deposited using composite targets in a DC magnetron sputtering system (Balzers Cube). A 4-inch Si wafer with a 1 μm thick SiO_2 layer was used as the starting structure, on which a 200 nm thick TiW bottom electrode was deposited and patterned. An insulating layer, comprising a 35 nm thick layer of SiO_2, was deposited and etched to form vias with diameters of 90 nm. The vias were filled with 35 nm thick GST to form the active phase-change region. Finally, a 200 nm thick TiW top electrode was deposited to complete the structure.

c. Electrical characterization

The electrical performance of the cells was investigated using an in-house-built PC device-testing system (26) comprising a picosecond (Picosecond Pulse Labs) or nanosecond (Tektronix) pulse generator, a digital oscilloscope (Agilent Technologies), and a probe station, as shown in SI Appendix: Fig. S2. The picosecond-pulse generator has the specifications of pulse durations ranging from 100 ps to 10 ns, rise time of 65 ps, and amplitude of 7.5 V, while the nanosecond-pulse generator has the specifications of pulse durations ranging from 5 ns to 900 ns, a rise time of less than 3 ns, and amplitude of 5 V. The cell is connected to the pulse generator and oscilloscope via low-capacitance cables (~0.2-3 pF) and a load resistor of $R_l = 50\ \Omega$. The upper limit of the time constant of the RC circuit is estimated to be ~several 10 ps.

The full-width, half-maximum (FWHM) time duration of the pulse was measured at V_{in}, and this was used to characterize the speed of switching in the PC cells. We have previously investigated and reported the waveform of the voltage pulses obtained at V_{in} and V_{out} (27). As in those studies, the waveform of the pulse obtained at V_{in} also reflects the exact voltage pulse that is applied to the cell, taking into account the capacitance or inductance of the probe, circuitry and connectors. The FWHMs of the waveforms measured at V_{in} and V_{out} are almost the same. In addition, as the signal measured at V_{out} has passed through the cell, the duration of the pulse experienced by the cell is almost identical to that of the pulse entering the cell. Furthermore, a comparison of the shapes of the pulses measured at V_{in} and V_{out} also shows that parasitic-capacitance effects in the circuit or cell are negligible (Figs. 1a, b, S3), and in the case where they exist near the end of the pulses, they dissipate in a time with an upper limit of a few ns, consistent with those reported by other groups

(28-30).

We have used one of the conventional cell structures employed by many other research groups (32,32). The pulse width needed to switch the cells via a single pulse using our present cell was found to be several tens of ns (depending on the voltage applied, see SI Appendix: Fig. S15), which is about the same as those achieved with other cells (33,34). This means that the effect of heat retention in our cells is similar to the other cells, and thereby confirms that the shorter pulse achieved via priming in this study is not affected arbitrarily by the cell structure employed, nor by its heat-retention properties.

The current flow in a cell is calculated via the voltage V_{out} probed at the bottom of the cell, and is defined by $I = V_{out}/R_l$. The length and amplitude of the electrical pulses were varied from several 100 ps to several 10 ns, and from 0 to 7 V, respectively. To ensure good functionality, the cells were switched reversibly more than 100 times between the low- and high-resistance levels of 0.05 and 1 MΩ before the experimental study.

d. Simulational procedure

The molecular-dynamics simulations were performed using the Vienna Ab initio Simulation Package (VASP) (35). The projector augmented-wave (PAW) method (36), with the Perdew-Burke-Ernzerhof (PBE) exchange-correlation functional (37), was used. The GST models were simulated in cubic supercells with periodic boundary conditions. The plane-wave energy cutoff was 174.98 eV. All the outer *s* and *p* electrons were treated as valence electrons. The time step in the simulation was fixed at 5 fs, and the temperature was controlled via a velocity-rescaling algorithm. The density used was 6.11 g/cm^3, chosen to be between the experimental amorphous- and

crystalline-phase densities of GST (38). Initial random atomic configurations were mixed at 3000 K, maintained at 1200 K for tens of ps, and then quenched to 300 K at a rate dT/dt = -15 K/ps to generate the amorphous configurations. The amorphous models were then annealed at 600 K for 500 ps to generate the crystalline configurations. To study the melting kinetics, the crystalline models were subjected to varying temperatures between 800 K and 900 K.

e. Structural characterization of the models

Based on structural motifs characteristic of the metastable rocksalt structure of crystalline GST, we studied the time evolution of structural units based on the number of fourfold rings in the model. Fourfold rings were defined when four atoms form a closed ring, with an average bond angle of 90°. A maximum deviation of +/-20° was allowed in the bond angle and in the plane angle between two parallel triangles (consisting of three atoms) that share a diagonal in the fourfold rings. Each ring, in principle, shares its four edges with four adjacent fourfold rings with an average inter-plane angle of 90°. A cut-off distance of R_{cut} = 3.5 Å between atoms was used to define these structural units.

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Author contributions

D.L., T.C.C., and S.R.E. designed the research; D.L., J.M.S., and W.J.W. performed the research; D.L., J.M.S., W.J.W., R.Z., and T.H.L. analyzed the data; and D.L., T.C.C., and S.R.E. wrote the paper, which incorporates critical inputs from all authors.

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Figure Captions

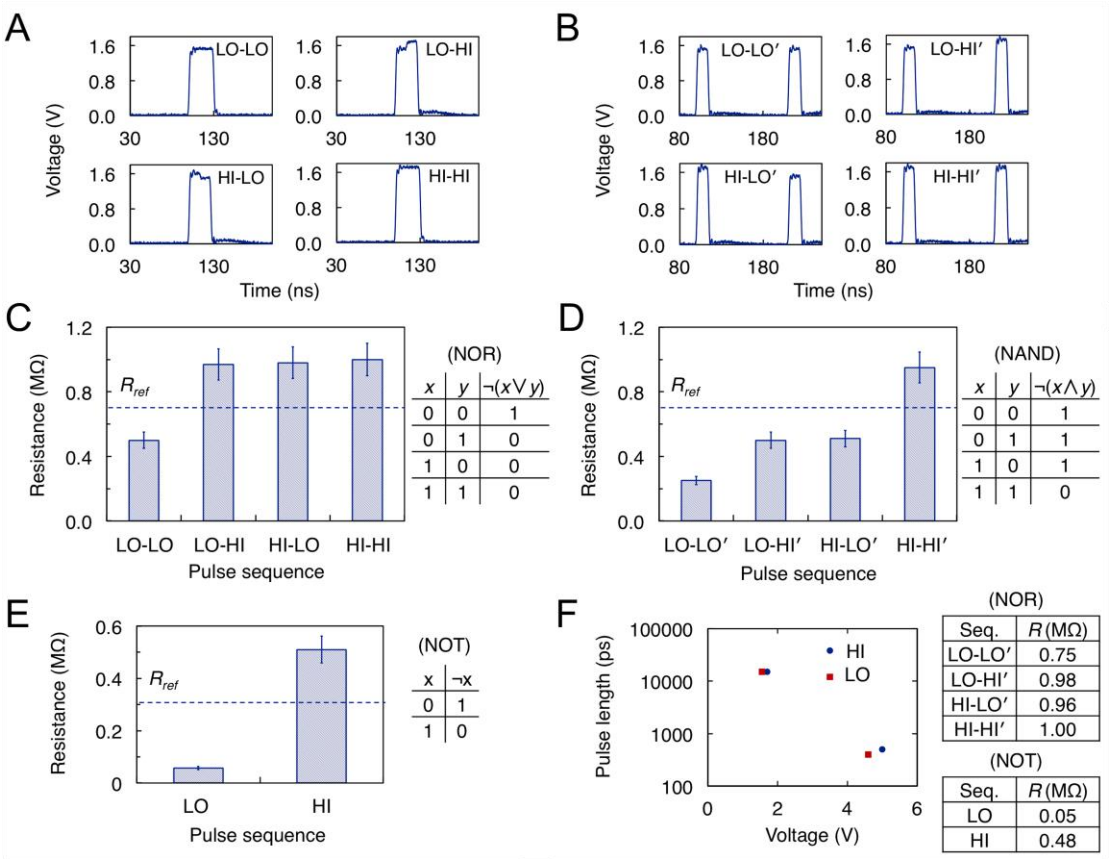
Figure 1. Examples of the use of *s*-to-*l* transitions for achieving fast and multiple Boolean algebraic (logic) operations in the GST cell. Waveforms for the double electrical-pulse sequence: **A)** without; and **B)** with a time separation between the pulses. The dependence of the electrical resistance on the 'double-pulse' excitation scheme applied to the cells used to demonstrate: **C)** $\neg(x \vee y)$/NOR and **D)** $\neg(x \wedge y)$/NAND operations, without and with ($'$) a separation between the pulses, respectively. **E)** Correlation between the electrical-resistance level and the single-pulse excitation employed to achieve the $\neg x$/NOT operation. HI and LO refer to high- and low-voltage pulses with amplitudes of V = 1.70 V and 1.55 V, respectively. The length of the pulses was kept constant at 15 ns, while the time separation between them, where required, was maintained to be the same at 100 ns. The reference resistance levels, R_{ref}, for the NOR and NAND, and NOT operations were chosen to be R = 0.7 MΩ and 0.3 MΩ, respectively. Truth tables for the Boolean algebraic operations are demonstrated (right of **C**-**E**). The HI and LO electrical pulses represent the binary numbers '1' and '0' for both inputs x and y of the Boolean algebraic operations, while the cell resistances below and above the R_{ref} values define the binary numbers '1' and '0' for the output of such operations, respectively. The error bars show the range of values obtained from experiments performed on three different cells. **F)** Plots showing the switching times achievable with different pulse voltages. (Right) The tables show the electrical-resistance values of the cells measured after applying picosecond-range pulses to perform NOR (top) and NOT (bottom) operations with a time separation between the pulses. The R_{ref} values for the NOR and NOT operations were chosen to be R = 0.8 MΩ and 0.3 MΩ, respectively. The cells

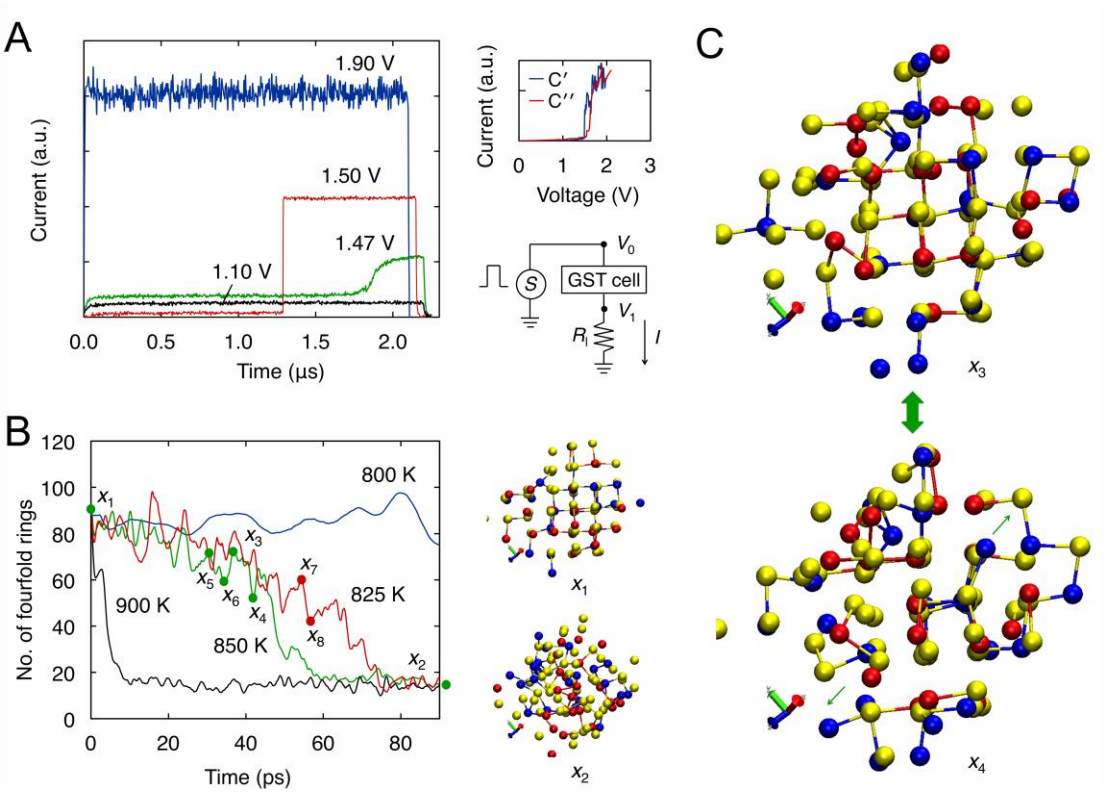
were switched between the low- and high-resistance levels of R = 0.05 and 1.00 MΩ, respectively.

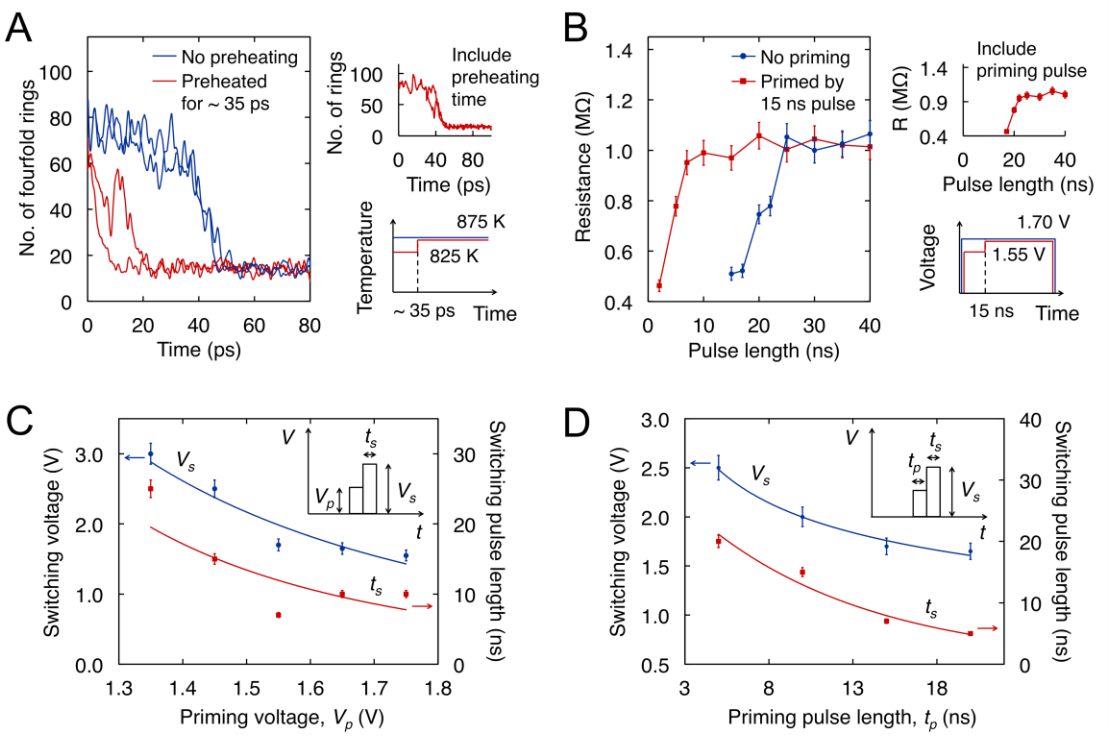
Figure 2. Experimental and simulational investigations of the origin and transience of the *s*-to-*l* transition in $Ge_2Sb_2Te_5$ (GST). A) Electrical-stimulus excitation of a GST cell. (Left) waveforms of the current flow, *I*, through the cell during pulsed excitation with V_0 = 1.10, 1.47, 1.50 and 1.90 V, and t = 2 μs. (Top right) DC current-voltage (*I*-*V*) characteristics of two different cells (C′ and C″). (Bottom right) schematics of the experimental set-up employed. *I* is calculated as the ratio between V_1 and R_l, with the former being the voltage measured at the bottom of the cell, and the latter being the resistance of the load resistor (50 Ω). V_0 is the voltage measured at the top of the cell. The cell exhibits an initial electrical-resistance level of R = 0.05 MΩ, while the final-resistance levels shown by the cell after the pulse excitations with the V_0 values listed above are R = 0.05, 0.30, 0.50 and 1.00 MΩ, respectively. **B)** *Ab initio* molecular-dynamics simulation of a GST model. (Left) time evolution of the number of fourfold rings in the model at T = 800, 825, 850 and 900 K. (Right) snapshots of the model at T = 850 K at the positions marked x_1 and x_2. **C)** Snapshots of the GST model at the positions marked x_3 and x_4 in (**B)**. Color coding of atoms: Ge, blue; Sb, red; Te, yellow. Bonds are shown between the atoms within a range of 3.5 Å. Snapshots of the GST model at configurations marked x_5 and x_6 are given in SI Appendix: Fig. S4, and those for configurations x_7 and x_8 in SI Appendix: Fig. S5.

Figure 3. Control and tuning of the *s*-to-*l* transition via the pre-melting disordering (PD) phenomenon in GST. A) Computer simulation of the PD

phenomenon in a GST model. (Left) time evolution of the number of fourfold rings in the preheated and non-preheated GST models melted at T = 875 K. The preheated model was heated at T = 825 K for two different times of t = 30 and 40 ps prior to the melting at T = 875 K, while the latter model was melted solely at T = 875 K from two different starting configurations. (Top right) overall melting process, including the evolution of rings during the initial thermal treatment of the preheated models (at T = 825 K for the two different times). (Bottom right) schematics of the heating profiles employed in the simulations. **B)** Electrical characterization of the PD phenomenon in a GST cell. (Left) Dependence of the electrical-resistance level of the primed and non-primed GST cells on the length of a switching pulse at V = 1.70 V. (Top right) complete switching scheme, but including the initial electrical stimulation applied to the primed cells with an electrical pulse of V = 1.55 V and t = 15 ns. (Bottom right) schematics of the electrical-pulse waveforms employed. Dependence of the pulse amplitude V_s and length t_s required to switch the cells on: **C)** the amplitude V_p and **D)** the length t_p of a priming pulse. V_p and V_s were kept constant at 1.55 V and 1.70 V, respectively, when the voltage dependence was not being investigated, while t_p and t_s were both maintained to be the same at t = 15 ns when not being employed as a variable. The error bars show the range of values obtained from the experiments performed on three different cells.


A
LO-LO
LO-HI
HI-LO
HI-HI
Voltage (V)
Time (ns)
B
LO-LO′
LO-HI′
HI-LO′
HI-HI′
Voltage (V)
Time (ns)
C
Resistance (MΩ)
R_{ref}
LO-LO
LO-HI
HI-LO
HI-HI
Pulse sequence
(NOR)
x | y | ¬(x∨y)
0 | 0 | 1
0 | 1 | 0
1 | 0 | 0
1 | 1 | 0
D
Resistance (MΩ)
R_{ref}
LO-LO′
LO-HI′
HI-LO′
HI-HI′
Pulse sequence
(NAND)
x | y | ¬(x∧y)
0 | 0 | 1
0 | 1 | 1
1 | 0 | 1
1 | 1 | 0
E
Resistance (MΩ)
R_{ref}
LO
HI
Pulse sequence
(NOT)
x | ¬x
0 | 1
1 | 0
F
Pulse length (ps)
HI
LO
Voltage (V)
(NOR)
Seq. | R (MΩ)
LO-LO′ | 0.75
LO-HI′ | 0.98
HI-LO′ | 0.96
HI-HI′ | 1.00
(NOT)
Seq. | R (MΩ)
LO | 0.05
HI | 0.48


A
1.90 V
1.50 V
1.47 V
1.10 V
Current (a.u.)
0.0 0.5 1.0 1.5 2.0
Time (μs)
Current (a.u.)
C′
C″
0 1 2 3
Voltage (V)
V_0
S
GST cell
V_1
R_l
I
B
120
100
80
60
40
20
0
No. of fourfold rings
800 K
900 K
850 K
825 K
x_1
x_2
x_3
x_4
x_5
x_6
x_7
x_8
0 20 40 60 80
Time (ps)
x_1
x_2
C
x_3
x_4


A
No. of fourfold rings
No preheating
Preheated
for ~ 35 ps
Time (ps)
No. of rings
Include
preheating
time
Time (ps)
Temperature
875 K
825 K
~ 35 ps
Time
B
Resistance (MΩ)
No priming
Primed by
15 ns pulse
Pulse length (ns)
R (MΩ)
Include
priming pulse
Pulse length (ns)
Voltage
1.70 V
1.55 V
15 ns
Time
C
Switching voltage (V)
Switching pulse length (ns)
Priming voltage, V_p (V)
D
Switching voltage (V)
Switching pulse length (ns)
Priming pulse length, t_p (ns)